**Arab Academy for Science and Technology**

**College of Language and Communication**

****

**Computer Architecture**

MIPS\_Single Cycle

(Report)

**Submitted by:** Abdelrahman Osama Elzarka

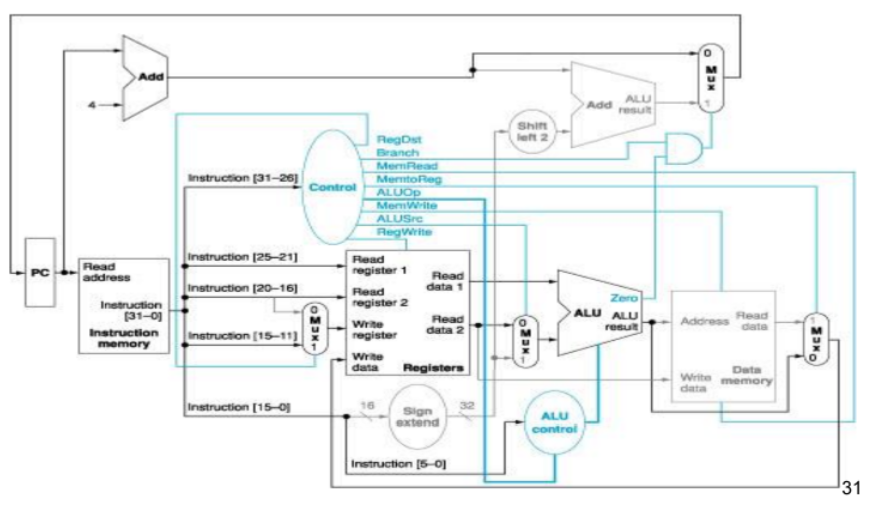
**Department:** computer engineering

**Reg #:** 19102262

**Submitted to:** Dr. Marwa & Eng. Samar

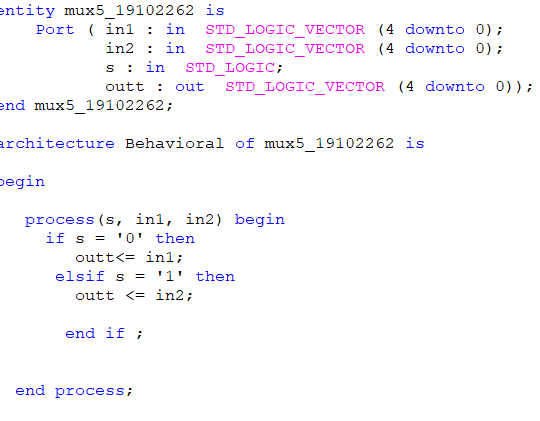
**Submitted on:** June 2, 2022

**The project’s structure**

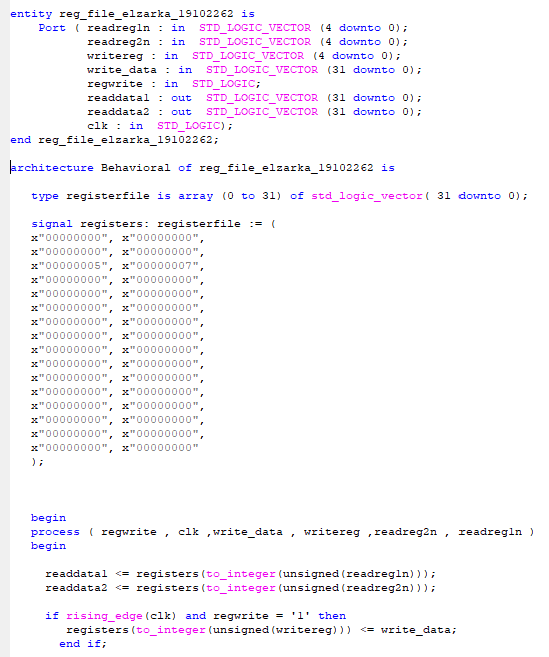
****

**The project consists of:-**

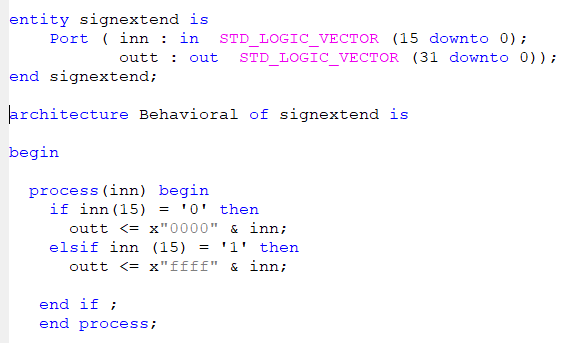
1- Mux 5 bits

****

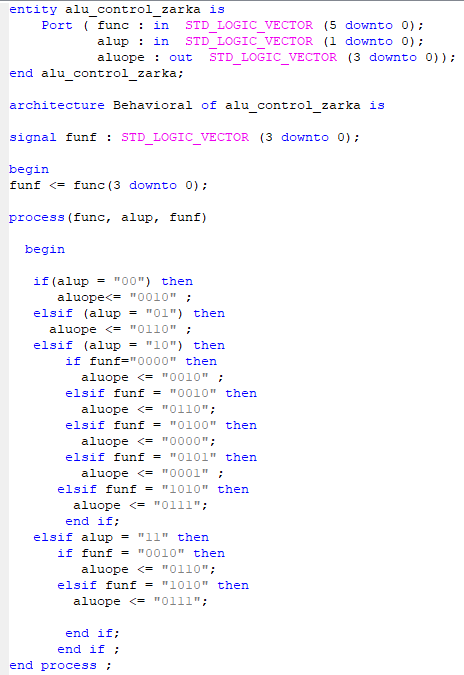
2- Registers file



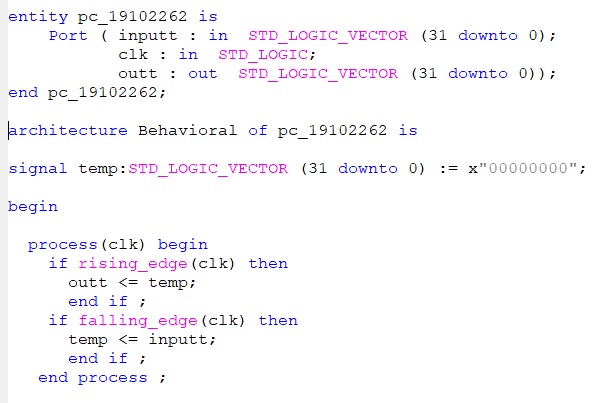
3- Sign extend



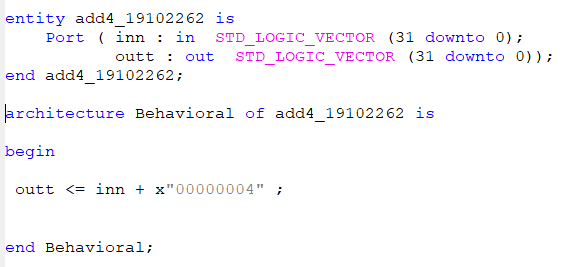
4- ALU control



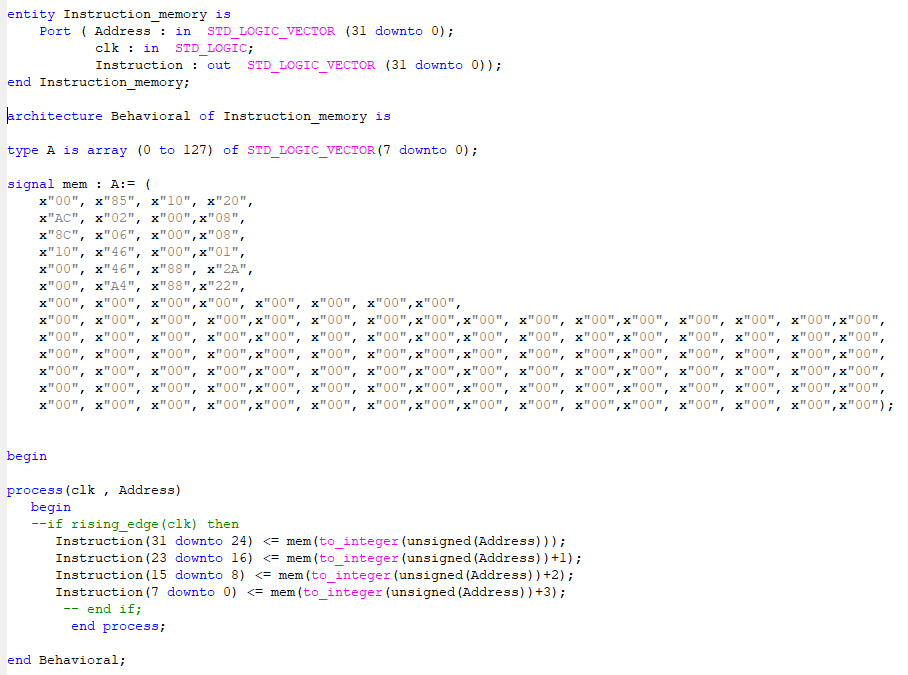
5- PC



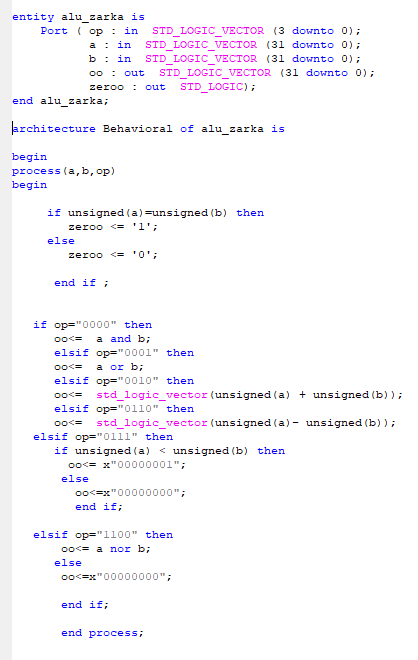
6- adder to number (4)



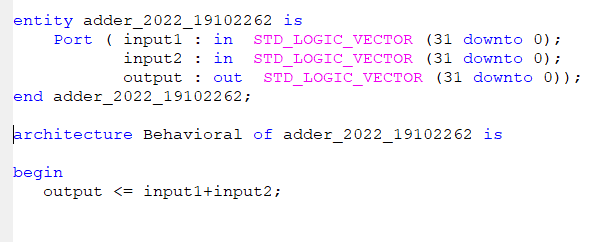
7- Instruction memory



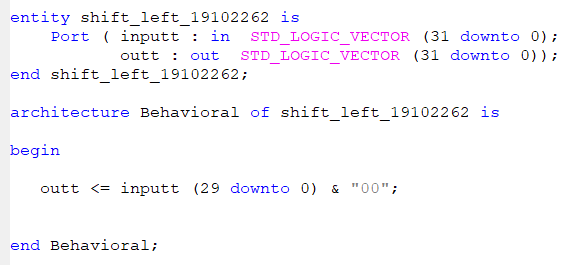
8- ALU



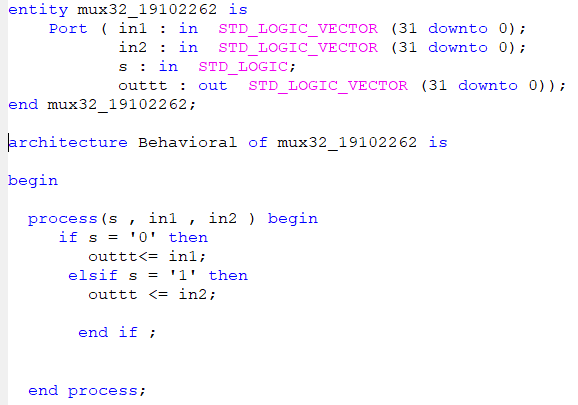
9- adder



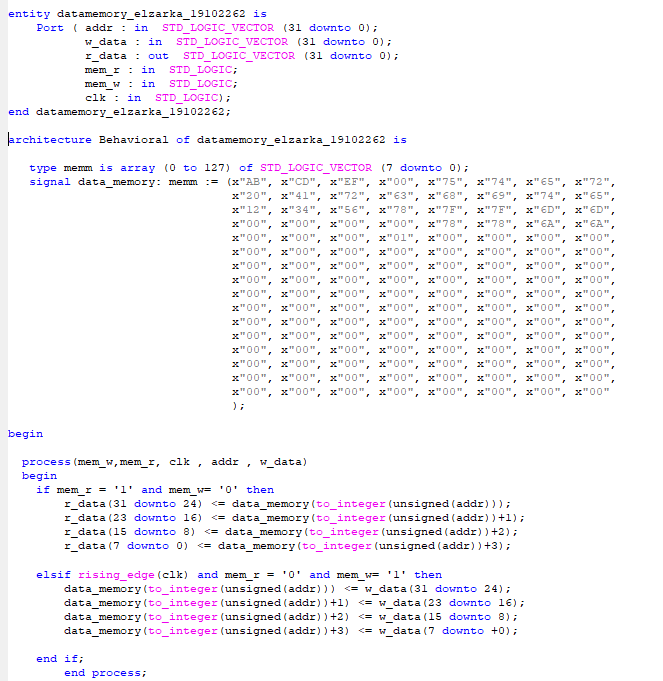
10- shift left



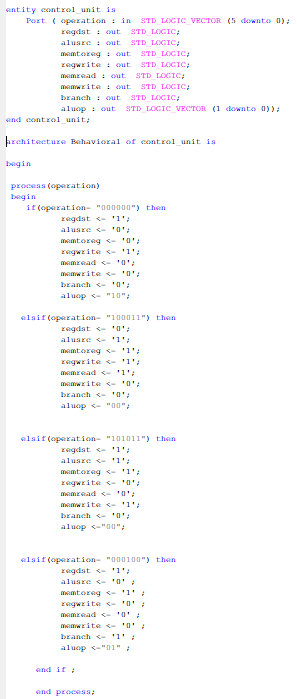
11- 3 mux 32 bit



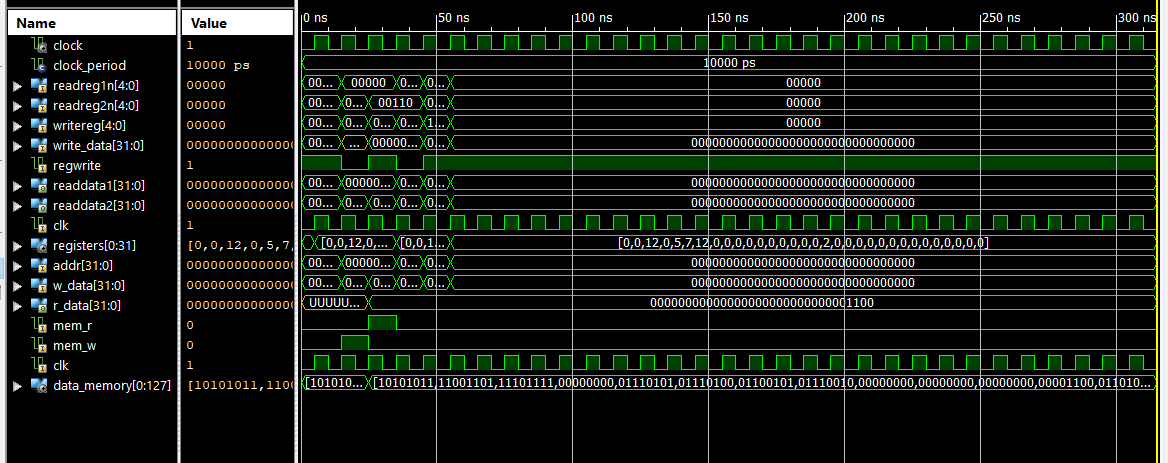
12- Data memory



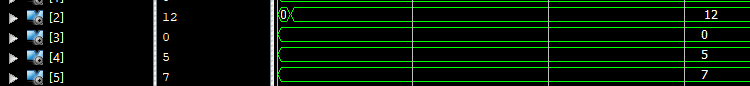
13- Control Unit



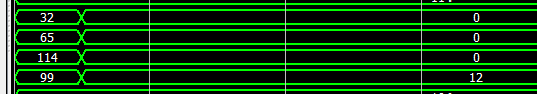
**The tested simulation:-**

****

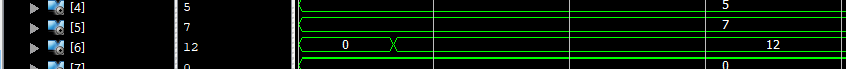
1. First clock : add $v0, $a0, $a1



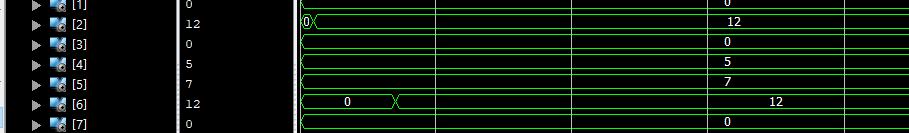
1. 2’s clock : sw $v0, 8($zero)



1. 3’s clock : lw $a2, 8($zero)



1. 4’s clock: beq $v0, $a2, Good\_Processor



1. 6’s clock : Good\_Processor: sub $s1, $a1, $a0

\*note 5’s clock with (SLT) will not be executed because V0 = a2 .